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10/730,002	12/09/2003	Raymond Jit-Hung Sung	9-16319-251US	2813

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,002	SUNG ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-16* is/are rejected.

7)☒ Claim(s) *17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the Amendment filed 11-30-2005.

Drawings

The drawings were received on 11-30-2005. These drawings are approved.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima (US PAT No. 3,999,081) in view of Kumar (US PAT No. 5,426,383).

Regarding claim 2, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches a single-rail multi-gate domino logic circuit (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30) driven by a multi-phase clock (Φ1, Φ2, Φ3) comprising: a first dynamic logic gate (Fig. 1d or Fig. 3a1) having an evaluate clock logic circuit (70 in Fig. 1d, 20 and 54 in Fig. 3a1) comprising at least p- channel first and second transistors (71,72 in Fig. 1d, 20 and 54 in Fig. 3a1) respectively driven by separate phases of the multi-phase clock, but does not teach the first and second transistors being n-type MOS FETs.

However, Fig. 10A and Fig. 10C of Kumar teaches a PMOS (25 in Fig. 10A) is replaced with NMOS (53 and 56 in Fig. 10C) using an inverter for the purpose of providing faster speed (col. 7, line 56+).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to replace a PMOS of Nakajima with a NMOS and an inverter of Kumar or vice versa for the purpose of variation in speed. It is also further noted that as a matter of engineering choice, it is well known in the art that a NMOS with the equivalent channel size as a PMOS provides higher driving current, so that it switches faster while a PMOS provides lesser threshold voltage.

Regarding claim 3, Nakajima in view of Kumar teaches the domino logic circuit as claimed in claim 2 wherein the first and second transistors are connected to perform any one of: a logical OR-function of a current clock phase and a next clock phase (when both of Φ1 & Φ2 are low, the output is low in Fig. 1d); a logical AND-function of a current clock phase and a previous clock phase.

Regarding claim 4, Nakajima in view of Kumar teaches the domino logic circuit as claimed in claim 2 wherein the dynamic logic stage further comprises a precharge clock logic circuit (53 in Fig. 3a1) having at least first and second n-channel transistors (51 & 52) driven by respective separate phases of the multi-phase clock signals (Φ1, Φ2), but does not teach the first and second transistors being p-type MOS FETs.

However, Fig. 10A and Fig. 10C of Kumar teaches a PMOS (25 in Fig. 10A) is replaced with NMOS (53 and 56 in Fig. 10C) using an inverter for the purpose of providing faster speed (col. 7, line 56+).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to replace an NMOS of Nakajima with PMOS using an inverter of Kumar for the purpose of variation in operating speed. It is also further noted that as a matter of engineering choice, it is well known in the art that a NMOS with the equivalent channel size as a PMOS provides higher driving current, so that it switches faster while a PMOS provides lesser threshold voltage.

Regarding claim 5, Nakajima in view of Kumar teaches the domino logic circuit as claimed in claim 2 wherein the first dynamic logic gate comprises any one of: an input complemented logic gate (Fig. 3a1 is a standard dynamic logic inverter); a non-monotonic logic gate; and a standard dynamic logic gate.

Regarding claim 6, Nakajima in view of Kumar teaches the domino logic circuit as claimed in claim 5, further comprising a plurality of logic phases connected in series, each logic phase comprising a respective first logic stage (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30, e.g. Fig. 3a1 may be coupled to any of Fig. 3b1 - 3f1) .

Regarding claim 7, Nakajima in view of Kumar teaches the domino logic circuit as claimed in claim 6, wherein at least one logic phase further comprises a second logic gate connected in series with the respective first dynamic logic stage (Figs. 1a-1f, 3a1-

3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30, e.g. Fig. 3a1 may be coupled to any of Fig. 3b1 - 3f1).

Regarding claim 8, Nakajima in view of Kumar teaches the domino logic circuit as claimed in claim 7, wherein the second logic gate comprises either one of: a static logic gate; and a standard dynamic logic gate (Figs. 3b1 - 3f1 are a standard dynamic logic gate).

Regarding claim 9, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches a single-rail domino circuit (Figs. 1a-1f, 3a1-3f1) driven in accordance with a multi-phase clock (Φ1, Φ2, Φ3), comprising: a plurality of logic phases connected in series (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 7, lines 60-65), each logic phase being respectively associated with a current clock phase (Φ1, Φ2, Φ3), and comprising at least one dynamic logic gate (Figs. 1a-1f, 3a1-3f1 are dynamic logic gate); a respective evaluate clock logic circuit (70 in Fig. 1d, 60 in Fig. 1b) connected to control an evaluate cycle of each logic phase, the evaluate clock logic circuit comprising respective first and second p-channel transistors respectively connected to receive one of a current clock phase (Φ1 in Fig. 1d, Φ3 in Fig. 1b) and an adjacent clock phase (Φ2 in Fig. 1d, Φ1 in Fig. 1b), such that overlap between a precharge cycle of a first logic phase and an evaluation cycle of an adjacent logic phase is prevented (Fig. 4), but does not teach the first and second transistors being n-type MOS FETs.

However, Fig. 10A and Fig. 10C of Kumar teaches a PMOS (25 in Fig. 10A) is replaced with NMOS (53 and 56 in Fig. 10C) using an inverter for the purpose of providing faster speed (col. 7, line 56+).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to replace a PMOS of Nakajima with a NMOS and an inverter of Kumar or vice versa for the purpose of variation in speed. It is also further noted that as a matter of engineering choice, it is well known in the art that a NMOS with the equivalent channel size as a PMOS provides higher driving current, so that it switches faster while a PMOS provides lesser threshold voltage.

Regarding claim 10, Nakajima in view of Kumar teaches a single-rail domino circuit as claimed in claim 9, wherein a first dynamic logic gate lies on a boundary between its respective logic phase and a previous logic phase (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30, e.g. Fig. 3a1 may be coupled to any of Fig. 3b1 - 3f1), and comprises any one of: an input complemented logic gate (Fig. 3a1 is a complementary, i.e. inverter dynamic logic gate); a non-monotonic logic gate; and a standard dynamic logic gate.

Regarding claim 11, Nakajima in view of Kumar teaches a single-rail domino circuit as claimed in claim 10 wherein the first dynamic logic gate is connected in series with a second logic gate (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30, e.g. Fig. 3a1 may be coupled to any of Fig. 3b1 - 3f1) within the

same logic phase (Φ1, Φ2, Φ3 in Fig. 4), the second logic gate comprising either one of: a static logic gate; and a standard dynamic logic gate (Fig. 3a1 is a complementary, i.e. inverter dynamic logic gate).

Regarding claim 12, Nakajima in view of Kumar teaches a single-rail domino circuit as claimed in claim 9, wherein the first and second n-channel transistors are connected to perform any one of: a logical OR-function of the respective current clock phase and a next clock phase (60 in Fig. 1b performs a logic OR function of Φ1, Φ3); a logical AND-function of the respective current clock phase and a previous clock phase.

Regarding claim 13, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches a single-rail domino circuit (Figs. 1a-1f, 3a1-3f1) driven in accordance with a multi-phase clock (Φ1, Φ2, Φ3), comprising: a first dynamic logic stage (Fig. 3a1) comprising a precharge clock logic circuit (53) comprising at least one n-mosfet transistor (51, 52) respectively driven by a separate phase of the multi-phase clock (Φ1, Φ2) and a second dynamic logic stage (Fig. 3d1) comprising an evaluate clock logic circuit (70) comprising at least one p-mosfet transistor (71,72) respectively driven by a separate phase of the multi-phase clock (Φ1, Φ2), but does not teach the precharge clock logic circuit comprising at least one p-mosfet transistor and the evaluate clock logic circuit comprising at least one n-mosfet transistor.

However, Fig. 10A and Fig. 10C of Kumar teaches a PMOS (25 in Fig. 10A) is replaced with NMOS (53 and 56 in Fig. 10C) using an inverter for the purpose of providing faster speed (col. 7, line 56+).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to replace a PMOS of Nakajima with a NMOS and an inverter of Kumar or vice versa for the purpose of variation in speed. It is also further noted that as a matter of engineering choice, it is well known in the art that a NMOS with the equivalent channel size as a PMOS provides higher driving current, so that it switches faster while a PMOS provides lesser threshold voltage.

Regarding claim 14, Nakajima in view of Kumar teaches the domino logic circuit as claimed in claim 13 wherein the first dynamic logic stage comprises two p-mosfet transistors (20, 54 in Fig. 3a1) driven by separate phases of the multi-phase clock (Φ1, Φ3).

Regarding claim 15, Nakajima in view of Kumar teaches the domino logic circuit as claimed in claim 13 wherein the second dynamic logic stage comprises two n-mosfet transistors (22, 73 in Fig. 3d1) driven by separate phases of the multi-phase clock (Φ1, Φ2).

Regarding claim 16, Nakajima in view of Kumar teaches the domino logic circuit as claimed in claim 13 wherein the first dynamic logic stage performs any one of an OR-

precharge function and a domino-precharge function (53 in Fig. 3a1 performs a domino-precharge function); and the second dynamic logic stage performs any one of an AND-evaluation function; an OR-evaluation function; and a domino-evaluate function (70 performs a domino evaluation function).

Allowable Subject Matter

Claims 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Nakajima teaches a clock-controlled gate circuit and Kumar teaches replacement of PMOS and NMOS, one of ordinary skill in the art would not have been motivated to modify the teaching of Nakajima and/or Kumar to further includes, among other things, the specific of dynamic gates directly coupled back-to-back at cell boundaries without intervening state gate where the dynamic logic gate performs a dynamic cascaded OR-precharge/domino evaluation function (claim 17) and a dynamic cascaded AND-evaluate function (claim 18), a secondary precharge network comprising at least one p-mosfet transistor driven (claim 19), and a secondary precharge network comprising two p-mosfet transistors (claim 20).

Response to Arguments

Applicant's arguments filed 11-30-2005 have been fully considered but they are not persuasive.

Applicant argues that Nakajima in view of Kumar teaches away from the instant invention since none of the circuits claimed includes an inverter. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Kumar reference teaches the replacement of PMOS with the NMOS or NMOS with PMOS where an inverter is used to convert the PMOS to NMOS or NMOS to PMOS for the purpose of providing speed variations (col. 7, line 56+). It is also further noted by the examiner that as a matter of engineering choice, it is well known in the art that a NMOS with the equivalent channel size as a PMOS provides higher driving current, so that it switches faster while a PMOS provides lesser threshold voltage. Applicant further argues that the purpose of using PMOS devices which is not addressed by Nakajima or Kumar. However, the examiner notes that applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on Monday-Thursday 5:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

2-21-2006